

# Ethernet Multi-Ring Microcode Module

Data Sheet  
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## PRODUCT DESCRIPTION

The Ethernet Multi-Ring microcode module is used to separate frames from different protocols into different buffer descriptor rings. The module supports the following protocols:

- ARP
- ICMP
- TCP
- NVP
- UDP
- IPv6
- IPv6OverIP

Frames from all other protocols are sent to the default BD ring.

Each ring has its specific event bit in the event and mask registers (FCCE/M). This enables the user to directly access the proper ring, and also to mask interrupts on a per ring basis.

The key benefits of this module are:

- Saves on Host processing time
- Enables the application to set up different priorities to different protocols
- Better memory usage (by using buffer pools of various sizes)

**Note:**

The module can be customized to meet specific requirements. For example, the user may wish to use different or add other L3/L4 protocols (e.g. RTP instead of NVP). This can be easily done prior to shipment. For more details please contact DoGav Systems.

## MODIFICATIONS REQUIRED

The traditional FCC Ethernet parameter RAM is extended to include two additional parameters:

1. Offset 0xFC – MultiRing Base: Offset of the MultiRing structure's base address (with respect to the Dual Port RAM).
2. Offset 0xFE – must be initialized to 56 (0x0038).

In addition, the RBASE parameter must be initialized to the default BD.

## MICROCODE VERSION

This microcode module is mask version dependent. The header file and the source provided contain a facility to select the proper version dependent module.

## USER OPTIONS

The rings can be located in external memory. However, if the user decides to place them on the DPRAM (which saves the microcode a DMA read), the upper half-word of the base pointer should be cleared, leaving only the offset in the lower half-word. Note that the current BD pointer should be initialized with a full 32bit actual value.

For each protocol, the user may decide if the selection is desired OR the frame of that particular protocol will be routed to the default BD ring. In that case, both pointers should be cleared (zero).

## HOW TO WORK WITH THIS PRODUCT

In addition to the conventional FCC Ethernet initialization module the user should also initialize the MultiRing structure and the two additional parameters.

The user should call the C-function *InstallUcode* (supplied either in source or object form) in order to install the module. This function should be called from the application only once, right after the Ethernet driver initialization.



**Notes:**

1. In older PQII revisions (HIP 3) the microcode module is installed in the “user DPRAM” portion. If the user intends to use this module with these versions, 2K bytes at the beginning of the DPRAM are not available for the application. Refer to the PQII user manual sub-section “Dual-Port RAM” of the Communications Processor Module Overview chapter.
2. The module requires 2KB of memory.

**ABOUT DOGAV SYSTEMS**

DoGav Systems is a leading provider of software and hardware consultancy and training services. It specializes in Freescale's processors, in particular the PowerQUICC family of communication processors. It has a proven track record of over 20 years supporting Freescale customers in developing market-leading products for the communications equipment market.

DoGav Systems is Freescale's most experienced and active microcode developer. Since receiving its license in 2000, it has developed numerous customized microcode packages for both small and large Freescale customers. These packages are now successfully deployed in commercial products. In addition, DoGav Systems also offers more than 30 off-the-shelf microcode products for the PowerQUICC I, PowerQUICC II, PowerQUICC III and PowerQUICC II Pro processors.

