

QUICCEngine DMA Emulation using Microcode

PRODUCT DESCRIPTION

This package applies to Freescale's QE based devices (e.g. MPC832x, MPC8360, MPC8568).

It provides a replacement to the on-chip DMA module, which lack the "End of Transfer" capability.

The microcode is managed and controlled by Frame Descriptors (a.k.a. Buffer Descriptors). H/W handshake is supported (e.g. SOT, EOT).

The package is ideal for proprietary FPGAs that stream data to the QE in order to be encapsulated into a supported protocol (e.g. Ethernet, ATM, TDM).

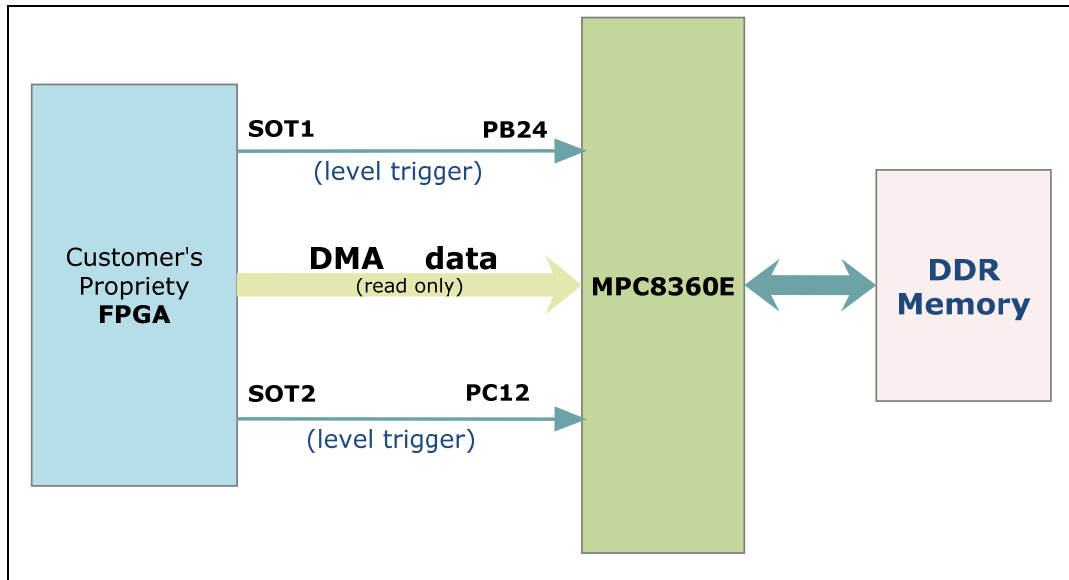
PRODUCT FEATURES:

Main features:

- Emulation of two DMA channels
- Offloads host (e300) core
- Dedicated (per channel) IO pins to trigger DMA transfer
- Level or edge triggered
- Configurable triggering polarity
- Configurable FPGA synchronization word (if desired)
- Dynamic frame length (per frame)
- Frame Descriptor (FD) oriented
- Supports FD chaining layout
- Generates interrupts on different events

The package can be further customised to specific customer requirements in order to offload the host and reach "interworking level".





Application example

Note:

This module has been successfully deployed in the field



ABOUT DOGAV SYSTEMS

DoGav Systems is a leading provider of software and hardware consultancy and training services. It specializes in Freescale's processors, in particular the PowerQUICC family of communication processors. It has a proven track record of over 20 years supporting Freescale customers in developing market-leading products for the communications equipment market.

DoGav Systems is Freescale's most experienced and active microcode developer. Since receiving its license in 2000, it has developed numerous customized microcode packages for both small and large Freescale customers. These packages are now successfully deployed in commercial products. In addition, DoGav Systems also offers more than 30 off-the-shelf microcode products for the PowerQUICC I, PowerQUICC II, PowerQUICC III and PowerQUICC II Pro processors.

