

IP/TCP/UDP CHECKSUM CALCULATION

Data Sheet

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PRODUCT DESCRIPTION

A microcode module aimed at significantly improving the performance of the Host processor to achieve higher overall system throughput. This module is only applicable to the FCC's Ethernet Protocol.

The module operates as follows:

- Incoming (Received) Frames:
 - If the incoming Ethernet frame is an IP frame, the IP header (L3) checksum is verified.
 - If the frame is a TCP or UDP frame, the L4 checksum is optionally verified.
- Outgoing (Transmitted) Frames:
 - Checksums are optionally calculated and inserted for L3 (IP) or/and L4 (TCP/UDP).

The checksum verification is employed on-the-fly for the receive direction. For the transmit direction the checksum is pre-calculated and inserted. If the user application can afford to allocate enough space on the DPRAM (size of larger Ethernet frame, subject to alignment restriction) the frame-reload is skipped.

ABOUT DOGAV SYSTEMS

DoGav Systems is a leading provider of software and hardware consultancy and training services. It specializes in Freescale's processors, in particular the PowerQUICC family of communication processors. It has a proven track record of over 20 years supporting Freescale customers in developing market-leading products for the communications equipment market.

DoGav Systems is Freescale's most experienced and active microcode developer. Since receiving its license in 2000, it has developed numerous customized microcode packages for both small and large Freescale customers. These packages are now successfully deployed in commercial products. In addition, DoGav Systems also offers more than 30 off-the-shelf microcode products for the PowerQUICC I, PowerQUICC II, PowerQUICC III and PowerQUICC II Pro processors.