

# I-TDM PROTOCOL 125 $\mu$ SEC MODE SUPPORT FOR THE QUICC ENGINE

(IN COMPLIANCE WITH PICMG SFP.1 [REV 1.0]).

## DATA SHEET

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## PRODUCT DESCRIPTION

This microcode module fully supports the I-TDM protocol in 125 $\mu$ sec mode on Freescale's QUICC Engine-based devices (e.g. MPC8360, MPC8568).

The microcode offloads a substantial amount of the processing resources from the host processor. The flow state machine as well as the individual I-TDM channel states are fully managed and maintained by the microcode.

The number of I-TDM channels is determined by the number of MCC channels supported by the specific QE implementation (i.e. 255 on the MPC8360 and MPC8568, 127 on the MPC8358 and 510 on the MPC8569).

The package includes microcode that should be installed on Freescale's IRAM. This customized microcode operates on MCC (TDM) ports as well as UCC (Ethernet) ports. It consists of three major modules:

- MCC to UCC (a.k.a. TDM to Packet) direction

- UCC to MCC (a.k.a. Packet to TDM) direction
- Host API which includes commands and events report (interrupts).

The microcode was developed in compliance with PICMG SFP.1 (rev 1.0).

Main features:

- Any MCC channel can be assigned to an I-TDM channel (as many as 255 to one I-TDM channel)
- Non-I-TDM channels can be configured to any MCC regular channel (HDLC, Transparent, SS7 etc.)
- Up to 8 flows (one per TDM port) are supported
- Any UCC can be assigned as an Ethernet port
- The I-TDM Ethernet port is still capable of communication with regular Ethernet frames
- Packetizing and unpacketizing operations are fully carried out by microcode; no host intervention is required
- Reaffirmation and Rate Integrity Check commands are carried out by  $\mu$ code.
- The host API is available to modify the channel state (New, Close, Relocate)
- Interrupts are generated to notify the host for success or failure of new link creation for both locally and remotely initiated links.
- There is built-in grooming support (the “close” command is automatically implemented as the “relocate” command)
- “Reliable Commands” are acknowledged by microcode
- The host has the ability to inspect activities through comprehensive statistic counters
- There is no need for special hardware. Existing TDM/Ethernet systems can use this microcode with no hardware modifications.
- Flow timing is generated by an application-selected channel (this channel cannot be implemented as a normal channel)

## **ABOUT DOGAV SYSTEMS**

DoGav Systems is a leading provider of software and hardware consultancy and training services. It specializes in Freescale's processors, in particular the PowerQUICC family of communication processors. It has a proven track record of over 20 years supporting Freescale customers in developing market-leading products for the communications equipment market.

DoGav Systems is Freescale's most experienced and active microcode developer. Since receiving its license in 2000, it has developed numerous customized microcode packages for both small and large Freescale customers. These packages are now successfully deployed in commercial products. In addition, DoGav Systems also offers more than 30 off-the-shelf microcode products for the PowerQUICC I, PowerQUICC II, PowerQUICC III and PowerQUICC II Pro processors.